Claims

What is claimed is:

1. A method of implementing a software breakpoint in a multiprocessor system having a plurality of processors each coupled to a main memory, each of the processors having an instruction cache associated therewith, the method comprising the steps of:

retrieving an instruction, for which the breakpoint is to be inserted, from a corresponding instruction address in the main memory;

inserting a breakpoint code at the instruction address in main memory; and

after the breakpoint code is executed by a given one of the processors, storing the retrieved instruction in the corresponding instruction cache for that processor and setting a use-once indicator associated with the instruction as stored in the corresponding instruction cache for that processor, wherein the use-once indicator, when set for the instruction as stored in the instruction cache, is operative via cache control logic to clear a validity indicator associated with the instruction after a single fetch of the instruction from the instruction cache, such that subsequent attempts by the given processor to access the instruction as stored in the instruction cache will cause the processor to retrieve the breakpoint code at the instruction address in main memory.

2. The method of claim 1 wherein the instruction cache includes a plurality of sets of instruction information, each corresponding to a particular instruction, a given one of the sets of instruction information comprising the validity indicator, the use-once indicator, an instruction tag, and instruction data.

3. The method of claim 1 wherein the instruction address comprises an instruction tag, an index and a block offset.

4. The method of claim 1 wherein the cache control logic is operative to compare portions of the instruction address to corresponding portions of instruction information as stored in the instruction cache and checks the validity indicator in determining if there is a hit or a miss between the instruction address and the instruction information as stored in the instruction cache.

5. The method of claim 1 wherein the use-once bit when set, being operative via the cache control logic to clear the validity indicator associated with the instruction as stored in the instruction cache after a single fetch of the instruction from the instruction cache, thereby automatically causes a miss between the instruction address and the instruction as stored in the instruction cache when the given processor attempts to retrieve the instruction from the instruction cache subsequent to the single fetch.

6. The method of claim 1 wherein the use-once indicator associated with the instruction comprises a single bit stored in a given set of the instruction cache.

7. The method of claim 1 wherein the validity indicator associated with the instruction comprises a single bit stored in a given set of the instruction cache.

8. The method of claim 1 wherein the instruction for which the breakpoint is to be inserted comprises an instruction having a noncacheable attribute associated therewith.

9. The method of claim 1 wherein at least a subset of the retrieving, inserting, storing and setting steps are implemented under the control of a debugger which interfaces with the multiprocessor system.

10. The method of claim 1 wherein the breakpoint code inserted at the instruction address in main memory comprises a debug opcode.

11. A multiprocessor system comprising:

a main memory; and

a plurality of processors each coupled to the main memory, each of the processors having an instruction cache associated therewith;

wherein an instruction, for which the breakpoint is to be inserted, is retrievable from a corresponding instruction address in the main memory;

wherein a breakpoint code is insertable at the instruction address in main memory; and

wherein subsequent to execution of the breakpoint code by the given processor, the retrieved instruction is stored in the corresponding instruction cache for that processor, and a use-once indicator associated with the instruction as stored in the corresponding instruction cache for that processor is set, wherein the use-once indicator, when set for the instruction as stored in the instruction cache, is operative via cache control logic to clear a validity indicator associated with the instruction after a single fetch of the instruction from the instruction cache, such that subsequent attempts by the given processor to access the instruction as stored in the instruction cache will cause the processor to retrieve the breakpoint code at the instruction address in main memory.

12. An article of manufacture comprising a machine-readable storage medium for storing one or more software programs for implementing a software breakpoint in a multiprocessor system having a plurality of processors each coupled to a main memory, each of the processors having an instruction cache associated therewith, wherein the one or more software programs when executed implement the steps of:

retrieving an instruction, for which the breakpoint is to be inserted, from a corresponding instruction address in the main memory;

inserting a breakpoint code at the instruction address in main memory; and

after the breakpoint code is executed by a given one of the processors, storing the retrieved instruction in the corresponding instruction cache for that processor and setting a use-once indicator associated with the instruction as stored in the corresponding instruction cache for that processor, wherein the use-once indicator, when set for the instruction as stored in the instruction cache, is operative via cache control logic to clear a validity indicator associated with the instruction after a single fetch of the instruction from the instruction cache, such that subsequent attempts by the given processor to access the instruction as stored in the instruction cache will cause the processor to retrieve the breakpoint code at the instruction address in main memory.